Computer systems for space flight applications require ever increasing amounts of computing power to enable (on-the-fly) processing of large data sets from sophisticated experiments and payloads, or even to perform real-time computation of safety-critical control commands. Without this, spacecrafts would be unable to perform complex docking maneuvers or landing approaches autonomously. Besides meeting high performance requirements, the on-board computer systems must also provide interfaces that allow their embedment in a spacecraft's redundant communications infrastructure or support redundant ports for instruments with very high data transfer rates in the gigabit range.

With this in mind, the Open Modular Avionics Architecture (OMAC4S) initiative is developing an architectural framework for future on-board computer systems to enable the modular integration of components (hardware and software) with different performance and functional characteristics into the avionics infrastructure of a spacecraft.

In order to demonstrate the features of the OMAC4S architecture, the project partners are developing a set of processing nodes. One processing node is based on the Intel Atom® processor with a triple modularity redundancy (TMR) architecture, the second is a dual modular redundancy (DMR) system with the high-end P4080 embedded multicore processor from Freescale and the third option is a LEON4-based system in single-lane configuration. Also implemented on the basis of 1 Gbps Time-Triggered Ethernet (TTE) technology is a redundant deterministic interconnect network that enables further computers and subsystems to be hooked up quickly and easily. In addition, the project is developing an I/O component that allows remote sensors to be connected to the computer system

The OMAC4S approach allows different operating systems. Currently, Linux, VxWorks and PikeOS are supported. PikeOS is the preferred operating system as it supports time and space partitioning on single core but also on multicore CPUs.

A cross platform middleware allows application developers to use the provided node resources in a standardized way. The system support services implement the domain specific services such as the Packet Utilization Standard (PUS) in the space domain.

The project is supported by the German Aerospace Center’s Space Administration with funding from the Federal Ministry for Economic Affairs and Energy.
Overview

The OMAC4S compliant high-reliability processor node is built around the LEON4-N2X fault tolerant quadcore processor, running at a system frequency of 150MHz. The microprocessor interfaces fast DDR-2 random-access-memory and FLASH banks for program memory. The form-factor of the computer board is a 3U-card according to the PICMG compactPCI serial standard. The connection to the OMAC4S infrastructure is made via the PCI-serial interface on the backplane connector. Debugging can be performed via standard interfaces accessible on the front panel.

Architecture

The HRPN node is integrated into the OMAC4S infrastructure via the interface board also used by the Intel Atom based TRM system. This card provides the translation between the TTEthernet avionics bus and the cPCIserial interface of the processor node. The OMAC4S infrastructure provides access to dual redundant TTEthernet switches via the system backplane.

About Us

At Airbus Defence and Space in Bremen we can look back on more than two decades of designing and manufacturing of computers for space applications. Our experience ranges from stand-alone boards up to complex data handling systems in single-lane and redundant configurations. The fault tolerant computers on ATV are part of our portfolio as well as payload electronics. Our capabilities also include manufacturing and qualification of electronics and wiring harnesses according to ECSS and IPC standards. To complete our systems, we can also provide software engineering, coding and testing as well as standardised service layers for Columbus and ExpressRack data interfaces. Ground Support Equipment, standardised enclosures and verification testing complete the list of our services.
Overview

The OMAC4S compliant fault-tolerant on-board computer developed by Fraunhofer FOKUS is based on the P4080, an 8-core CPU from Freescale's QorIQ PowerPC multicore family. The processor can be operated at a clock speed of up to 1.5 GHz, thus theoretically reaching a maximum speed of approximately 60 GIPS (giga instructions per second). The P4080 processor benefits from the low-power silicon-on-insulator (SOI) technology, which is also less radiation-sensitive than conventional CMOS technology. The project has validated the system's lower radiation sensitivity to the total ionizing dose (TID) and single event upsets (SEUs) in a number of irradiation tests. The SOI technology is also largely latch-up-free. Furthermore, the P4080 offers the advantages of a highly integrated embedded processor: all important functions are already integrated on-chip, which made it possible to implement an entire compute node on a single 3U cPCI® Serial board.

Architecture

Despite the SOI technology's low radiation sensitivity, the conditions encountered in space mean that sporadic radiation-induced faults in the P4080 processor and the other COTS based components of a compute node cannot be ruled out. In order to meet, nonetheless, the high reliability and availability requirements for space systems, effective fault tolerance mechanisms are essential at all levels of a COTS-based computer system. The P4080-based high-performance computer is configured as a dual modular redundancy (DMR) system. It consists of two identical compute nodes with a shared I/O backplane. The OMAC4S specific interfaces, e.g. TTEthernet were implemented with suitable IPs as part of an radiation hard FPGA on the mission specific I/O backplane.
Overview

The OMAC4S compliant Remote Data Concentrator is versatile building block to connect legacy devices and other simple hardware sensors or actors to a TT Ethernet network. The Remote Data Concentrator provides an TT Ethernet slave interface at 100 MBit/s. To connect simple devices the Remote Data Concentrator provides 32 general purpose digital I/O lines (GPIO), 7 analogue input lines, 2 analogue output lines 8 pulse width modulated output lines and two pulse counter inputs. Further a redundant CAN interface and two UARTs are provided.

Architecture

The Remote Data Concentrator consists of a central FPGA accompanied by a multitude of interface ICs to provide the electrical adaption of the interfaces to the FPGA. For complex control operations and protocol handling the a Leon3 softcore CPU can be used. Several IP cores are provided to support the data acquisition on the analogue interfaces and to provide the TT Ethernet slave functionality on top of IEEE Ethernet.
Overview

The OMAC4S compliant TTEthernet switch TTESwitch 12-port cPCI-Serial is a high-speed deterministic Ethernet switch enabling critical network-centric applications. The high-performance switch enables packet processing at all twelve ports with full line speeds. It supports the three different open standards IEEE 802.3-2005, SAE AS6802 and ARINC 664 part 7 and further allows to synchronize the whole network to sub-microsecond jitter in a fault-tolerant manner.

TTEthernet technology allows to conveniently configure the switch during system design time for deterministic processing of critical (time-triggered, rate-constrained) and non-critical Ethernet traffic.

Benefits

The system architecture in current spacecraft is typically divided into an avionics sub-system which is, depending on the mission safety- or mission-critical, and a payload sub-system handling high-speed, non-critical (sensor) data. New mission scenarios and the evolution of technology are leading to new requirements on both the avionics- and the payload sub-system with respect to increase performance, determinism, reliability and availability. This requires a technology which is able to provide a cost competitive solution for both sub-systems. The OMAC4S standard provides a flexible, scalable and modular platform which is able to deal with these upcoming challenges. It makes use of technologies based on open standards deployed cross-industry which increases the performance, reduces the overall system complexity and reduces lifecycle costs.

The use of TTEthernet as communication network enables the integration of the avionics and the payload sub-system on the same physical media without an impact on mission critical systems or on the safety of the mission itself. Using one infrastructure for both sub-systems leads to a significant reduction of complexity and would moreover lead to significant savings in size, weight and power while increasing the performance of the overall system.
PikeOS is a real-time operating system (RTOS) designed for safety and security critical applications. PikeOS provides ARINC-653 compliant time and space partitioning. The operating system is DO-178B certified and used to provide robust partitioning for DO-297 Integrated Modular Avionics (IMA) devices. With PikeOS application software of different safety levels and security domains can be executed on a single platform.

PikeOS is available for the most popular processor architectures like x86, ARM, PowerPC and Sparc. Single and multi core CPUs are supported. Multi core systems can be configured for both Symmetric Multi Processing (SMP) and Asymmetric Multi Processing (AMP).

PikeOS provides integrated hypervisor functionality. It is capable of concurrently running different APIs, runtime environments and guest operating systems in separated partitions. Available are: PikeOS native API, ARINC 653 APEX, POSIX, Linux, Android, AUTOSAR, Real-time Java, Ada, RTEMS

PikeOS is the first and only operating system that has achieved the highest possible certification level for usage on a multi core platform. The operating system has been certified according to multiple safety standards like DO-178B, IEC 61508 and EN 50128. It is used in many different industrial devices that provide safety and security critical functions in real time.

Architecture

PikeOS uses a modular architecture with well defined internal interfaces. Therefore modules can be added, removed or customized for the individual project’s needs. The heart of PikeOS is a microkernel. The kernel comes with some processor family specific code which is in the Architecture Support Package (ASP). In addition a Platform Support Package (PSP) provides the code required to run the selected embedded device. All other PikeOS modules are executed in non-privileged modes of the CPU. The PikeOS system software (PSSW) contains all necessary means to manage the system and provides the PikeOS native programming API.

Within up to 62 partitions software based on different APIs, runtime environments and guest operating systems can be used.
KARS (Controller for autonomous spacecraft) is a versatile application framework for on-board software. It provides basic services widely used in the space domain. This includes data management and monitoring (DM), housekeeping reporting, event and event-action handling (EVH), logging (LOH), basic equipment handling (EQH), interface to the command and control channel (IOH) based on the Packet Utilization Standard (PUS), execution of on-board control procedures (OBCP) and mission timelines (MTH). The strict component based approach supports the easy integration of third-party components such as Attitude and Orbit Control System (AOCS), Thermal Control System (TCS), etc.

An Operating System Abstraction Layer allows porting to different operating systems with minimal effort. Currently, Linux, PikeOS and VxWorks are supported as standard. Board support packages are available for Intel, ARM, Leon3FT and Leon4 CPU boards. The development of the software has been performed according to the strict rules of the ECSS-E40. A full set of documentation is available to support certification activities.

## Architecture

### Overview

**Architecture**
Overview

The environment for validation of operational concepts consists of three elements: an OMAC4S compliant processing node incl. DLR’s KARS application framework, the orbit simulation with 3D visualization capabilities (Orbiter 2010), and ground station software for monitoring and control of KARS via Packet Utilization Standard (PUS) messages.

The orbit simulator provides realistic orbit simulation. Different mission scenarios can be configured and executed in real-time. Equipment models can be added easily by a simple plugin mechanism.

A network interface allows to exchange data between the simulator and the OMAC4S compliant processing node on-board computer (OBC) model. The OBC model is based on an OMAC4S compliant processing node incl. the KARS application framework installed. The KARS framework provides full PUS support. In addition, functionalities can be added easily by on-board control procedures (OBCP) based on LUA scripts. In the example shown below the Attitude and Orbit Control System (AOCS), the Thermal Control System (TCS) and the Power Control and Distribution Management Unit (PCDU) are implemented as OBCPs. The OBCP execution can be controlled via corresponding PUS messages.

The provided software for monitoring and control provides a graphical interface to visualize the received housekeeping data and to send PUS commands to the OBC.

Architecture