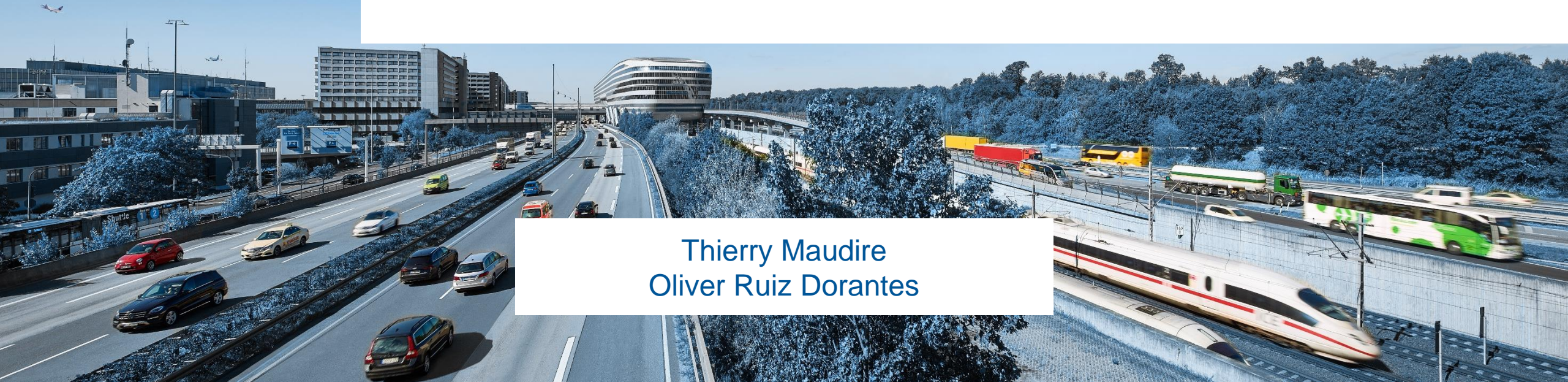




USE OF HETEROGENEOUS COMPUTING SYSTEMS AND PARTITIONED OPERATING SYSTEMS IN SPACE APPLICATIONS

Thierry Maudire
Oliver Ruiz Dorantes



Introduction

- Heterogeneous computer systems
- Operating systems
- Types of processing elements
 - General purpose: MMU vs MPU

Use Case

- HCS in Space applications
- SYSGO's PikeOS
- SYSGO's PikeOS for MPU
- Example architecture
- Conclusion



HETEROGENEOUS COMPUTER SYSTEMS (HCS)

A Heterogeneous Computing System (HCS) is a system that utilizes multiple different processing elements

General-Purpose processors (GPPs)	Digital Signal Processor (DSP)
Field-Programmable Gate Arrays (FPGAs)	Neural Processing Units (NPU)
	Graphics Processing Units (GPUs)

Advantages

- **High Performance:** Distribute workload among multiple specialized processing elements
- **Flexibility:** Different processing elements for different tasks
- **Robustness:** Implicit redundancy
- **Energy Efficiency:** Designed for specific tasks, turned on or off as needed

Partitioned Operating Systems (OS) are a type of operating system that allows multiple applications or tasks to run simultaneously on the same computing system. While also maintaining a **degree of isolation** between them.



- **Fault Isolation and Containment:** Each application or task is isolated from the others.
- **Resource Allocation:** Ability to allocate resources to specific applications or tasks.
- **Security:** Can prevent unauthorized access to sensitive data or the allocated resources.
- **Real-Time Performance:** Respond to events in a timely and deterministic manner.
- **Ease of Maintenance:** Each partition can be maintained independently.

PROCESSING ELEMENT TYPES

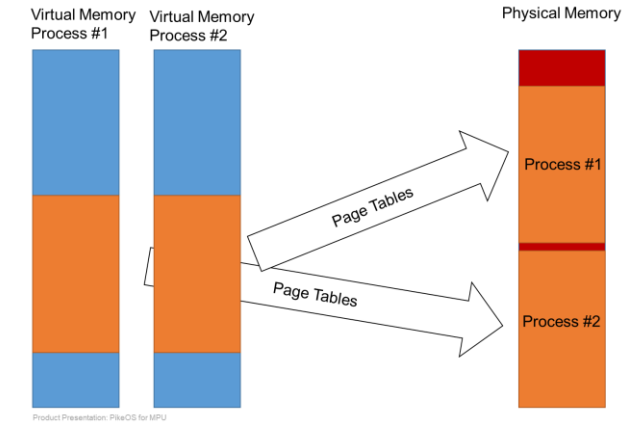
General-Purpose Processors (GPPs)	Digital Signal Processor (DSP)
Field-Programmable Gate Arrays (FPGAs)	Neural Processing Units (NPU)
	Graphics Processing Units (GPUs)

- **DSP:** Processing Audio Image Video Image Speech
- **NPU:** Neural network ...
- **GPU:** Graphics 2D/3D acceleration, float vectorial units
- **FPGA:** Custom Flexible HW IP
- **General-Purpose Processors (GPPs)**
 - Microprocessor MMU-based
 - Microcontroller MPU-based

DIFFERENCES BETWEEN MMU & MPU?

- **M**emory **M**anagement **U**nit

- Translation of Virtual to Physical Memory
- Exposes a large address space dedicated to a single process.
- Each chunk of virtual memory (called page) can be mapped to a page in linear physical memory
- Allows complex operating systems with multiple independent processes



- **M**emory **P**rotection **U**nit

- There is exactly one linear physical address space
- All processes share the same address space
- Found in less complex CPUs such as microcontrollers

Physical Memory



- Less complex
- More deterministic
- SEU events
- Faster boot
- Lock step

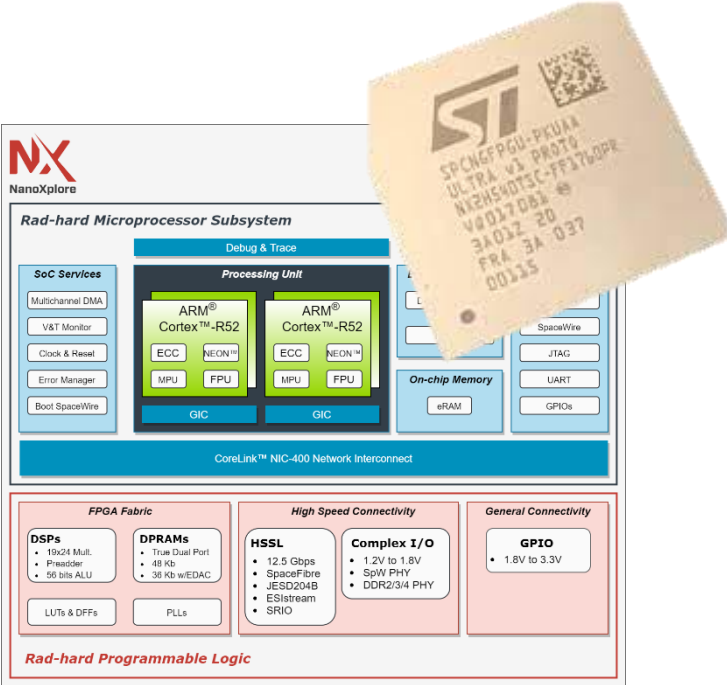
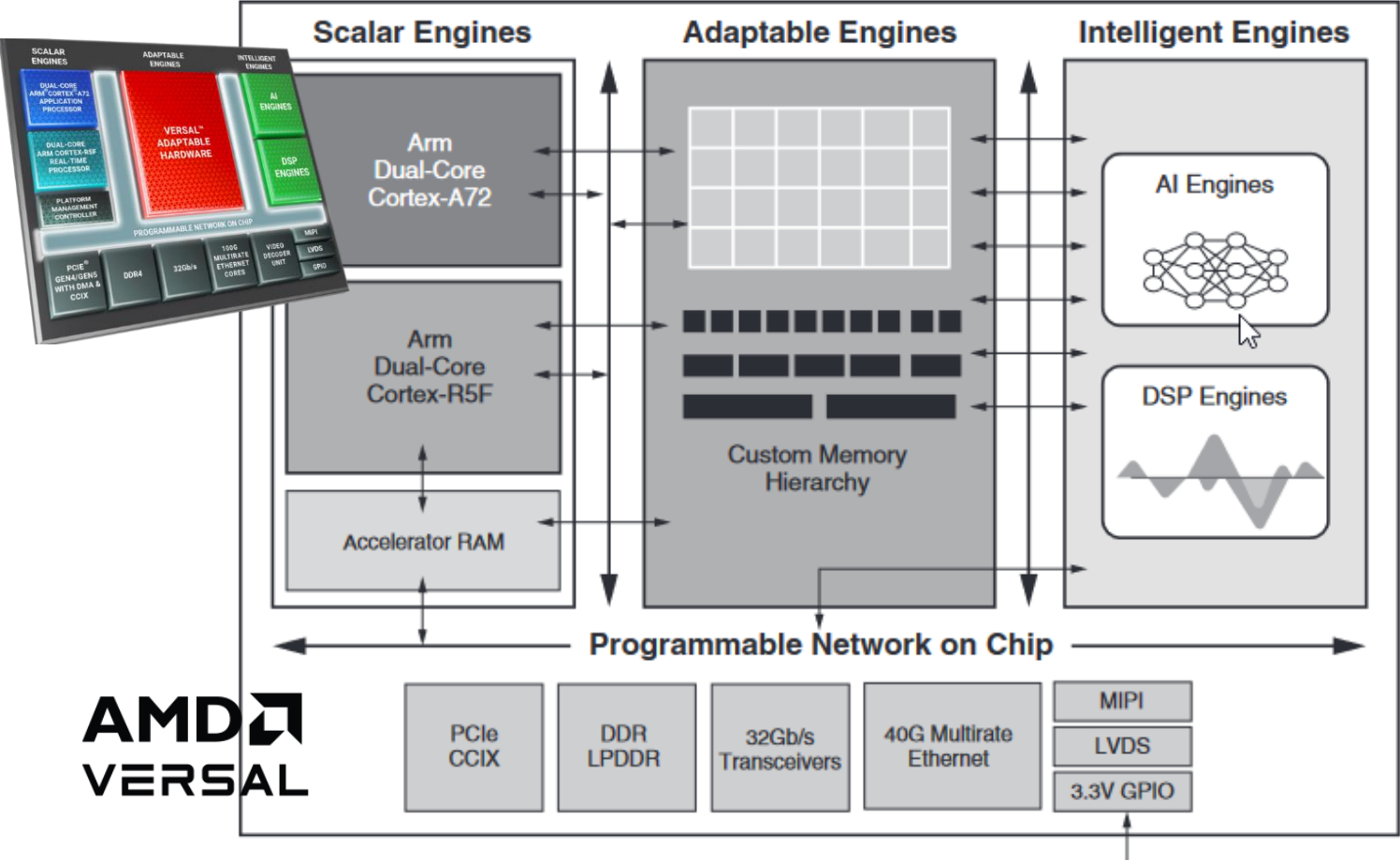


USE CASE

SYSGO PIKEOS AND XILINX VERSAL



THE HW PLATFORM



Xiphos Q8S	AMD-Xilinx Zynq Ultrascale+ MPSOC Quad-core ARM Cortex-A53	Nano-, Micro-, and SmallS
Innoflight CFC-400	AMD-Xilinx Zynq Ultrascale+ MPSoC Quad-core ARM Cortex-A53	CubeSat
Novo Space SBC002AV	quad A53 + dual R5 (Xilinx Zynq Ultrascale+)	General Satellite
KP Labs Leopard	AMD Xilinx Zynq UltraScale+ MPSoC; Quad ARM Cortex-A53 CPU; Dual ARM Cortex-R5 in lock-step	CubeSat

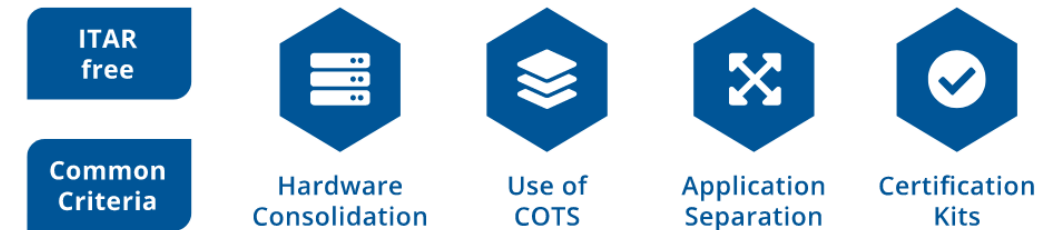
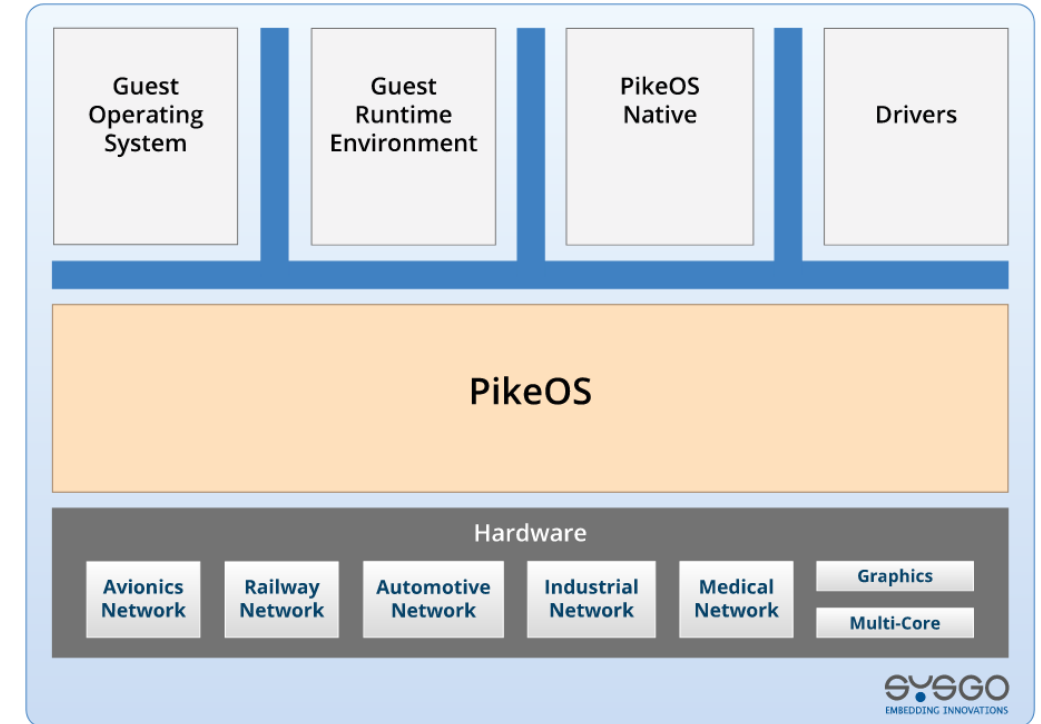
PIKEOS - CERTIFIED RTOS & HYPERVISOR

PikeOS

- RTOS and Hypervisor in one product
- Wide range of guest partitions / operating systems (POSIX, ARINC, Linux, Android, AUTOSAR, ...)
- Combined Safety and Security in a single product with mixed criticality
- Broad support of hardware architectures x86, ARM, PPC, RISC-V
- Certifiable to highest Safety and Security standards

Reduction of Time-to-Market

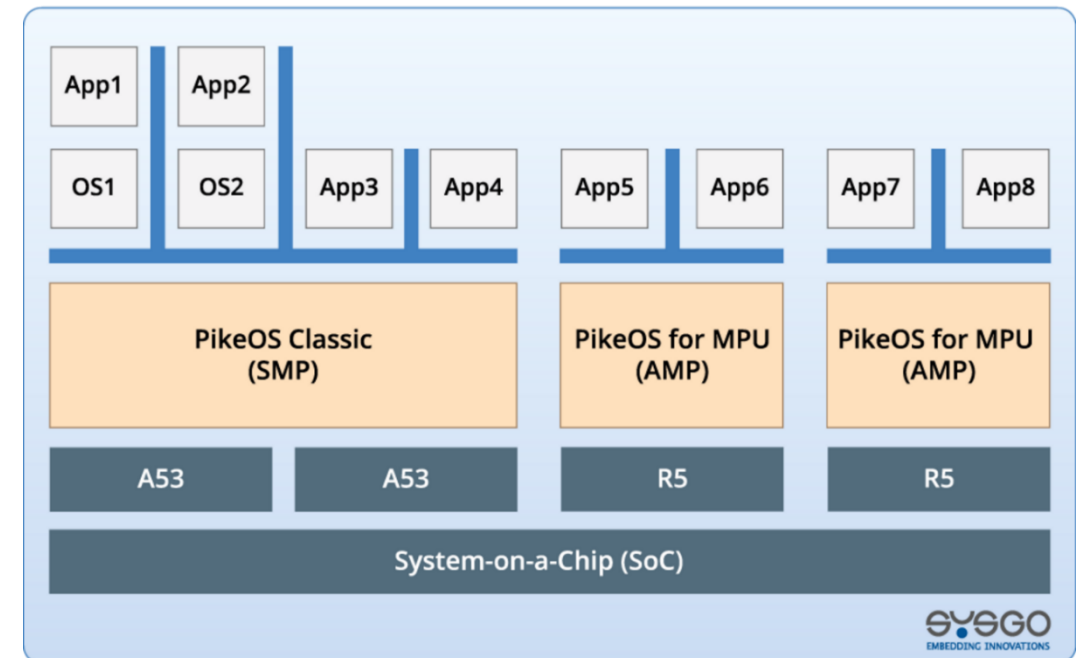
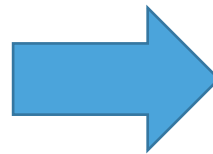
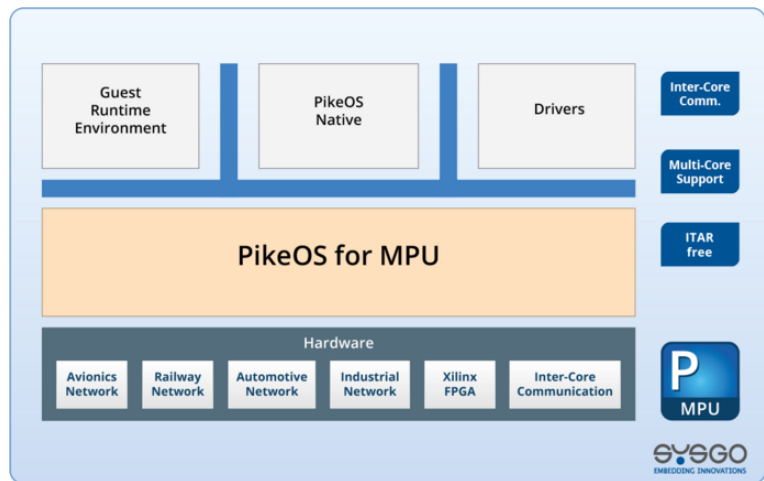
- Seamless hosting of third party applications
- Easy project configuration
- Certification artefacts
- Without any export restriction



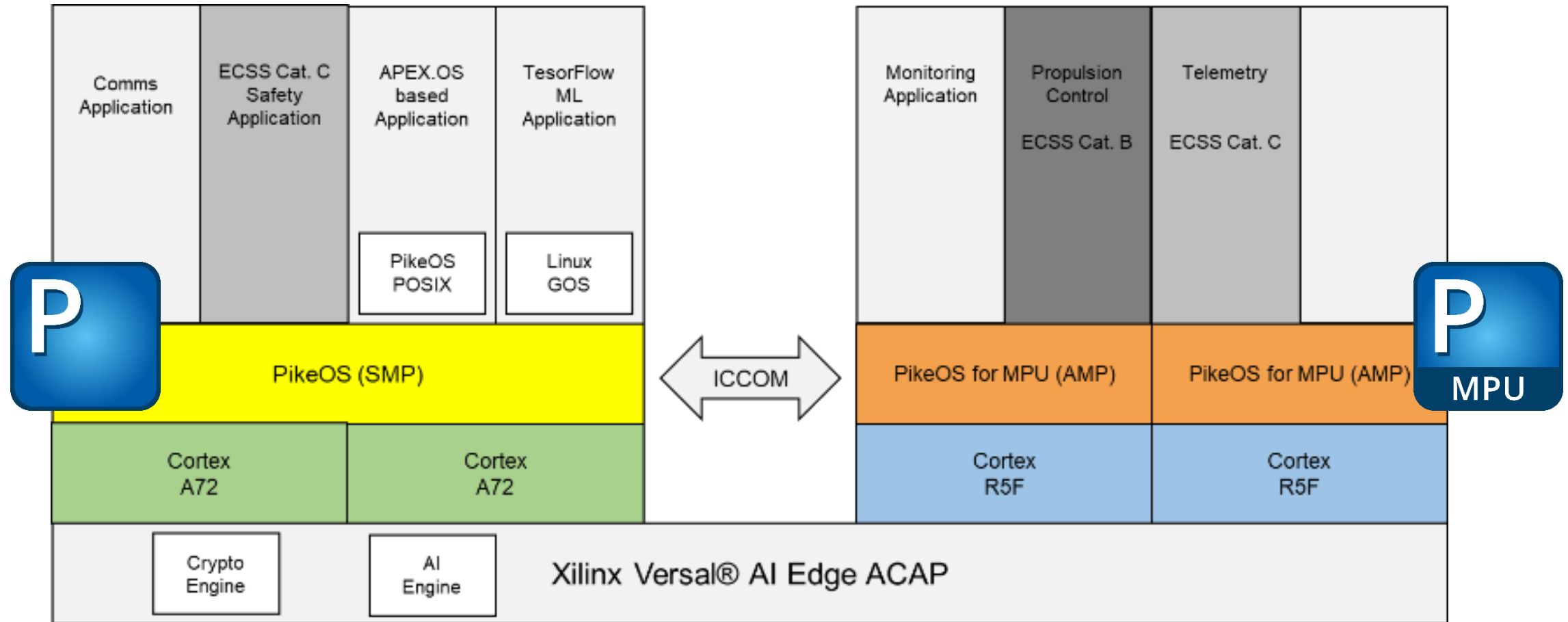
PIKEOS FOR MPU

PikeOS for MPU

- Reuses most of PikeOS code base, and provides the same API
- Targeted to MPU based CPU cores
- Architected around a AMP Separation kernel
- Configurable mechanism for communication between AMP cores created (Inter-Core Communication (ICCOM))



EXAMPLE USE CASE ARCHITECTURE



- The use of heterogeneous computing platforms offer the highest level of integration and miniaturization to achieve low SWaP footprints.
- The level of specialization offered by such heterogenous HW architecture must not be offset by the use of inadequate software platforms
- SYSGO PikeOS & PikeOS for MPU allows the integration & consolidation:
 - Distribute the satellite SW functions to the specialized units
 - Ensuring the appropriate level of functional safety and cyber-security
 - Fulfill the strict hard real time behavior

QUESTIONS OR COMMENTS?

SYSGO GmbH

Am Pfaffenstein 8
55270 Klein-Winternheim
Germany

Phone: +49 6136 99480
E-Mail: info@sysgo.com

Sales Contact
sales@sysgo.com

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